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UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte HUY THANH VO

Appeal 2007-3606
Application 09/808,750
Technology Center 2800

Decided: April 17, 2008

Before KENNETH W. HAIRSTON, JOSEPH F. RUGGIERO, and CARLA M. KRIVAK, *Administrative Patent Judges*.

KRIVAK, *Administrative Patent Judge*.

DECISION ON APPEAL

Appellant appeals under 35 U.S.C. § 134 (2002) from a final rejection of claims 1-41 and 45-57. We have jurisdiction under 35 U.S.C. § 6(b) (2002).

We affirm-in-part.

STATEMENT OF CASE

Appellant's claimed invention includes a memory array, memory device, integrated circuit, information handling device, and method of reducing wordline resistance-capacitance (RC) time constant by providing "a strapping line of lower resistance than the wordlines coupled to a single continuous wordline in a single array" (Br. 7). The strapping lines (low resistivity metal layers) can be attached to alternating halves of wordlines, can begin and end at various locations on the wordline as long as the pitch is sufficiently wide, and can be added to alternating wordlines in each array (Spec. 3:23 – Spec. 4:11).

Claims 1, 14, and 55, reproduced below, are representative of the subject matter on appeal.

1. A memory array, comprising:

a number of memory cells having a first source/drain region and a second source/drain region and a gate region;

a number of source lines coupled to the first source/drain region of at least one memory cell;

a number of bit lines coupled to the second source/drain region of at least one memory cell;

a number of wordlines coupled to the gate region of at least one memory cell;

a strapping line of lower resistance than the wordlines coupled to a single continuous wordline in a single array, wherein the strapping line bypasses only a portion in a middle region between a first and second end of

the single continuous wordline, wherein the strapping line is spaced apart from adjacent conductive structures by a distance greater than a wordline pitch, and wherein the strapping line bypasses only a portion of a wordline within the single memory array and bypasses a different portion of a wordline within the single array than an adjacent strapping line; and

at least two channels connecting the strapping line to a first and second end of the portion of the single continuous wordline.

14. The memory device of claim 8 wherein the strapping devices strap a first half portion of a number of even wordlines in the array and a second half portion of a number of odd wordlines.

55. A memory device comprising:
a memory array including a number of memory cells;

an even row decoder located on a first side of the memory array;

an odd row decoder located on a second side of the memory array;

a single column decoder connected to the memory array;

a number of parallel wordlines local to the memory array coupled to gate regions of memory cells, including one or more even wordlines coupled to the even row decoder, and one or more odd wordlines coupled to the odd row decoder, the odd wordlines arranged alternately with the even wordlines; and

a number of strapping lines having lower resistance than the wordlines and connected to bypass portions of the wordlines within the memory array, wherein a strapping line connected to an odd wordline bypasses only a portion of the odd wordline within the memory array nearer the odd row decoder, wherein a strapping line connected to an even wordline bypasses

only a portion of the even wordline within the memory array nearer the even row decoder.

REFERENCE

Cowles	US 5,940,315	Aug. 17, 1999

The Examiner rejected claims 1-41 and 45-57[1] under 35 U.S.C. § 102(b) based upon the teachings of Cowles.

Appellant contends that the Examiner did not make out a prima facie case of anticipation because Cowles does not teach each and every element recited in the claims (Br. 11). Particularly, Cowles does not show "a number of memory cells," "a number of source lines," and "a number of bit lines" (Br. 12; cls. 1, 5, 8, 15, 19, 26, 30, 37, 45, 49, and 55). In addition, Cowles does not recite an even row decoder on a first side of a memory array and an odd row decoder on a second side of a memory array (Br. 18; cl. 55).

ISSUE

Did the Examiner present a prima facie case of anticipation of claims 1-41 and 45-57 under 35 U.S.C. §102(b)?

FINDINGS OF FACT

1. Appellant's claims recite a number of memory cells, a number of wordlines coupled to at least one memory cell, and a strapping line of

[1] Claims 42-44 were cancelled by the Amendment of March 10, 2004.

lower resistance than the wordlines coupled to a single continuous wordline in a single array (cl. 1).

2. The strapping line bypasses only a portion in a middle region between a first and second end of the single continuous wordline and bypasses a different portion of an adjacent strapping line (cl. 1).

3. In a single memory array the strapping devices strap "a first half portion of a number of even wordlines in the array and a second half portion of a number of odd wordlines" (cl. 14).

4. Cowles teaches that every other row decoder block in a semiconductor memory device is eliminated by providing a metal layer strap across every other wordline in each array (col. 2, ll. 46-50).

5. Cowles teaches that each memory array includes "a plurality of memory cells (not shown)" (col. 3, ll. 27-29).

6. Cowles also teaches that although the straps are shown as "spanning the entire respective memory array, the invention is not so limited and straps 110-115 may span any portion of the respective memory arrays" (col. 3, ll. 57-60).

7. Fig. 1 of Cowles shows an arrangement where an even row decoder is on one side of two memory arrays and an odd row decoder is on the opposite side of the two memory arrays.

PRINCIPLES OF LAW

In rejecting claims under 35 U.S.C. § 102, a single prior art reference that discloses, either expressly or inherently, each limitation of a claim

anticipates that claim. *Perricone v. Medicis Pharmaceutical Corp.*, 432 F.3d 1368, 1375-76 (Fed. Cir. 2005), citing *Minn. Mining & Mfg. Co. v. Johnson & Johnson Orthopaedics, Inc.*, 976 F.2d 1559, 1565 (Fed. Cir. 1992).

The law of anticipation, however, does not require that the reference teach what the Appellant is claiming, but only that the claims at issue "read on" something disclosed in the reference. *See Atlas Powder Co. v. IRECO, Inc.*, 190 F.3d 1342, 1346 (Fed. Cir. 1999); *Kalman v. Kimberly-Clark Corp.*, 713 F.2d 760, 772 (Fed. Cir. 1983).

ANALYSIS

Claims 1-13, 15-41, and 45-53

Appellant has provided substantially the same arguments for each of the claims. Thus, as an initial matter, our decision is with respect to claim 1 which is representative of the independent claims. Turning to the rejection, the Examiner indicated how the claimed invention is deemed to be fully met by the disclosure of Cowles (Ans. 3-17). Appellant countered that Cowles does not teach each and every element of Appellant's claimed invention. Particularly, Cowles does not teach a "number of memory cells," "a number of source lines," and a "number of bit lines" (Br. 12). Appellant asserts that the Examiner has not produced the proper intrinsic evidence to show that these elements are present in Cowles (Br. 12).

Cowles teaches a strapped wordline architecture for a semiconductor memory device such that every other row decoder block in a semiconductor memory device is eliminated by providing a metal layer strap across every other wordline in each array (FF 4). Cowles also teaches that each memory array includes "a plurality of memory cells (not shown)" (FF 5). Memory cells, by Appellant's own definition (Spec. 3:18-19; Spec. 6:1-7; Fig. 4), include a transistor having a gate region, a source region and a drain region, bit lines and source lines. Thus, these limitations regarding the memory cells, source lines and bit lines "read on" Cowles.

Appellant also asserts that Cowles teaches that the conductive straps "bypass a wordline across an entire memory array" (Br. 12) instead of only a "portion of a wordline within the single array" (Br. 12; cls. 1, 5, 8, 15, 19, 26, 30, 37, 45, 49, and 55) as claimed by Appellant. Cowles, however, does teach that, although the straps are shown as "spanning the entire respective memory array, the invention is not so limited and straps 110-115 may span any portion of the respective memory arrays" (FF 6). Thus, the broad claim language reads on Cowles. Independent claims 5, 8, 15, 19, 26, 30, 37, 45 and 49 all recite similar limitations to claim 1 and Appellant provides the same arguments with respect to these claims. For the reasons set forth above, these claims, in addition to dependent claims 6, 7, 9-13, 16-18, 20-25, 27-29, 31-36, 38-41, 46-48, and 50-53, are anticipated by Cowles.

Claims 14 and 54-57

Claims 14 and 54 depend from claims 8 and 49, respectively, and recite that in a memory device that includes a single array the strapping devices strap a first half portion of a number of even wordlines in the array and a second half portion of a number of odd word lines in the array. Cowles does not teach nor suggest this arrangement of strapping lines over even and odd wordlines including first and second half portions, respectively. Thus, claims 14 and 54 do not read on Cowles.

With respect to claim 55, the Examiner asserts that he considers the arrays of Cowles as a single array (Ans. 19). The Examiner, however, has provided no basis for this reasoning. Rather, as Appellant correctly states Cowles shows an arrangement where an even row decoder is on one side of *two* memory arrays and an odd row decoder is on the opposite side of the *two* memory arrays (Fig. 1; FF 7) (emphasis added). Thus, a row decoder is used for multiple arrays reducing the number of decoders required for a memory bank (Abstract). Claim 55 recites an even row decoder located on a first side of *the* memory array and an odd row decoder located on a second side of *the* memory array (Br. 18) (emphasis added). Claim 55 also recites that in the memory array, "a strapping line connected to an odd wordline bypasses only a portion of the odd wordline within the memory array nearer the odd row decoder" and "a strapping line connected to an even wordline bypasses only a portion of the even wordline within the memory array nearer the even row decoder." Cowles does not disclose this structure recited in claim 55 (Br. 18). Thus, claim 55 does not read on what is disclosed by

Cowles and is not anticipated by Cowles. Because claims 56 and 57 depend from claim 55, we find that Cowles also does not anticipate these claims.

CONCLUSION

We therefore conclude that the Examiner did not err in rejecting claims 1-13, 15-41, and 45-53, under 35 U.S.C. §102(b). We also conclude that the Examiner did err in rejecting claims 14 and 54-57 under 35 U.S.C. §102(b).

DECISION

The decision of the Examiner rejecting claims 1-13, 15-41, and 45-53, is affirmed and the decision of the Examiner rejecting claims 14 and 54-57 is reversed.

No time period for taking any subsequent action in connection with this appeal may be extended under 37 C.F.R. § 1.136(a)(1)(iv).

AFFIRMED-IN-PART

gvw

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